III B.Tech - II Semester – Regular / Supplementary Examinations APRIL 2024

VLSI DESIGN

(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours

Code: 20EC3603

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.

2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

			BL	СО	Max. Marks		
UNIT-I							
1	a)	Describe the Verilog HDL source code for a	L2	CO1	7 M		
		data flow modelling of 4 to 1 multiplexer					
		circuit and draw the relevant logic diagram.					
	b)	Design module of 4 bit counter and a test	L3	CO1	7 M		
		bench for the same using always construct.					
	OR						
2	a)	Design a full adder using half adder	L3	CO1	7 M		
		modules and an OR gate. Write a Verilog					
		code using gate level modelling.					
	b)	Develop a verilog module of 2 x 4 decoder	L3	CO1	7 M		
		using data flow modeling.					

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Max. Marks: 70

		UNIT-II			
3	a)	Implement 2-input AND and OR logic	L3	CO2	7 M
		functions using FPGA.			
	b)	Describe the operation of CPLDs and their	L2	CO2	7 M
		Internal Architecture.			
		OR			
4	a)	Illustrate the different programmable logic	L3	CO2	7 M
		devices and basic programming block in			
		each PLD.			
	b)	Describe the necessity of CPLD and FPGA	L2	CO2	7 M
		to design the digital circuits.			
		UNIT-III			
5	a)	Describe the CMOS fabrication using	L2	CO3	7 M
		N-well process with detailed steps and			
		relevant diagrams.			
	b)	Compare the NMOS, CMOS and GaAs	L4	CO3	7 M
		Technologies.			
		OR			
6	a)	Differentiate the enhancement mode and	L4	CO3	7 M
		depletion mode of NMOS with diagrams.			
	b)	Apply the Moore's Law of IC? Briefly	L3	CO3	7 M
		outline the CMOS fabrication methods.			
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	T	UNIT-IV	1	· · · · ·	
7	a)	Derive the I_{DS} - V_{DS} relationship of an	L4	CO3	7 M
		NMOS transistor and explain the various			
		operating regions.			

b)Realise the layout of CMOS inverter.L3CO37 M0R0Apply the Lambda (λ)-based design rules for wires, contacts and Transistors.L3CO37 Mb)Analyze the working of NMOS Inverter with relevant diagrams.L4CO37 MUNIT-V9a)Why scaling is required? Derive the scaling factors for different types of device parameters.L4CO410 Mb)Illustrate the concept of Switch logic with relevant examples.L3CO44 MORIDa)Examine the limitations of Scaling in VLSI design.L4CO410 Mb)Design a 2:1 MUX using pass transistor only and explain its operation.L3CO44 M		1	1						
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