PVP 20

Code: 20EC3603

III B.Tech - II Semester – Regular / Supplementary Examinations
APRIL 2024

VLSI DESIGN
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

			BL	CO	Max. Marks
		UNIT-I			
1	a)	Describe the Verilog HDL source code for a data flow modelling of 4 to 1 multiplexer circuit and draw the relevant logic diagram.	L2	CO1	7 M
	b)	Design module of 4 bit counter and a test bench for the same using always construct.	L3	CO1	7 M
		OR			
2	a)	Design a full adder using half adder modules and an OR gate. Write a Verilog code using gate level modelling.	L3	CO1	7 M
	b)	Develop a verilog module of 2 x 4 decoder using data flow modeling.	L3	CO1	7 M

UNIT-II					
3	a)	Implement 2-input AND and OR logic functions using FPGA.	L3	CO2	7 M
	b)	Describe the operation of CPLDs and their Internal Architecture.	L2	CO2	7 M
OR					
4	a)	Illustrate the different programmable logic devices and basic programming block in each PLD.	L3	CO2	7 M
	b)	Describe the necessity of CPLD and FPGA to design the digital circuits.	L2	CO2	7 M
UNIT-III					
5	a)	Describe the CMOS fabrication using N-well process with detailed steps and relevant diagrams.	L2	CO3	7 M
	b)	Compare the NMOS, CMOS and GaAs Technologies.	L4	CO3	7 M
OR					
6	a)	Differentiate the enhancement mode and depletion mode of NMOS with diagrams.	L4	CO3	7 M
	b)	Apply the Moore's Law of IC? Briefly outline the CMOS fabrication methods.	L3	CO3	7 M
UNIT-IV					
7	a)	Derive the I_{DS} - V_{DS} relationship of an NMOS transistor and explain the various operating regions.	L4	CO3	7 M

	b)	Realise the layout of CMOS inverter.	L3	CO3	7 M
OR					
8	a)	Apply the Lambda (λ)-based design rules for wires, contacts and Transistors.	L3	CO3	7 M
	b)	Analyze the working of NMOS Inverter with relevant diagrams.	L4	CO3	7 M
UNIT-V					
9	a)	Why scaling is required? Derive the scaling factors for different types of device parameters.	L4	CO4	10 M
	b)	Illustrate the concept of Switch logic with relevant examples.	L3	CO4	4 M
OR					
10	a)	Examine the limitations of Scaling in VLSI design.	L4	CO4	10 M
	b)	Design a 2:1 MUX using pass transistor only and explain its operation.	L3	CO4	4 M